

# High-voltage GaN-HEMT devices, simulation and modelling

Stephen Sque, NXP Semiconductors ESSDERC 2013 Bucharest, Romania 16<sup>th</sup> September 2013

### Outline

- GaN and related materials
- The AlGaN/GaN heterostructure
- GaN wafers
- GaN devices
- Issues facing high-voltage GaN-HEMT development
- High-voltage breakdown
- GaN-HEMT device simulation
- Compact modelling of GaN HEMTs
- Summary and conclusion



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# Gallium nitride

• Gallium nitride (GaN) is a binary III-V compound material, with:

- Wurtzite (hexagonal) crystal structure
- Wide band gap of 3.4 eV (direct)
- High thermal conductivity







# **Properties of GaN**

Selected properties at 300 K:

Property	Si	4H-SiC	Diamond	GaAs	GaN
Band gap (eV)	1.1	3.2	5.5	1.4	3.4
Relative permittivity	11.9	10	5.5	12.5	9–10
Breakdown field (MV/cm)	0.3	3	5	0.4	3
Thermal conductivity (W/K/cm)	1.48	3.30	20.00+	0.54	1.30



# **Aluminium nitride**

- Aluminium nitride (AIN) is a binary III-V compound material, with:
  - Wurtzite (hexagonal) crystal structure
  - Wide band gap of 6.2 eV (direct)
  - High thermal conductivity







### AlGaN

- Take GaN and replace a fraction *x* (the *mole fraction*) of the Ga atoms with AI atoms  $\Rightarrow AI_xGa_{1-x}N$
- Most material properties are then intermediate between those of GaN and AIN

Quantity	GaN	Al <sub>0.2</sub> Ga <sub>0.8</sub> N	AIN	Units	Interpolation
Band gap	3.43	3.77	6.20	eV	Bowed, factor -1.33
Breakdown field	3.3	4.32	8.4	MV/cm	Linear (?)
Relative permittivity	9.5	9.3	8.5		Linear

[R. Quay, Gallium Nitride Electronics, ISBN 978-3-540-71890-1]



# **GaN crystal growth**

- Convention: [0001] direction
   is along *c* axis from Ga to N
- A-face: atom of type A is on top of bilayer
- Single-bond (low energy) surface



[O. Ambacher et al., J. Appl. Phys. 85 (6), 3222 (1999)]



# **Polarisation**

**Ga-face** 



Substrate

- Ga–N bonds are *polar*
- The Wurtzite crystal structure is non-centrosymmetric (*i.e.*, it lacks inversion symmetry)
- Result: spontaneous
   polarisation of the material

♦ E
Net internal electric field
Polarisation

**Note:**  $P_{SP}$  of AIN is stronger than that of GaN

[O. Ambacher et al., J. Appl. Phys. 85 (6), 3222 (1999)]



[E. T. Yu *et al.*, J. Vac. Sci. Technol. B **17 (4)**, 1742 (1999)] PUBLIC 9

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# **Piezoelectric effect**

- Applying stress to the material distorts the crystal structure, causing further polarisation: piezoelectric polarisation P<sub>PE</sub>
  - If the horizontal lattice parameter *a* is varied from its natural value *a*<sub>0</sub> there will be non-zero piezoelectric polarisation along the vertical (*c*) axis:





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### The AIGaN/GaN heterostructure

- AIN has a smaller lattice constant a<sub>0</sub> than GaN
- …and more spontaneous polarisation P<sub>SP</sub>
- Grow  $AI_xGa_{1-x}N$  on top of (relaxed) GaN:





# The AIGaN/GaN heterostructure

- Electronic band gap of AIN is larger than that of GaN
  - The band gap of Al<sub>x</sub>Ga<sub>1-x</sub>N is somewhere in-between
- Electrons confined to a thin region near the Al<sub>x</sub>Ga<sub>1-x</sub>N/GaN interface
- This is the two-dimensional electron gas (2DEG)
  - Areal density ~10<sup>13</sup> electrons/cm<sup>-2</sup>
- No doping ⇒ no impurity scattering
   ⇒ very high mobility





# Formation of the 2DEG

- Where do the electrons for the 2DEG "come from"?
- Model: donor-like surface states "provide" electrons

Electrons can come from Ohmic contacts. Surface donors play a role in the electrostatics.



[J. P. Ibbetson et al., Appl. Phys. Lett. 77 (2), 250 (2000)]



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### **GaN** wafers

Choice of substrate is very important

- Sapphire (Al<sub>2</sub>O<sub>3</sub>)
  - © Semi-insulating, can withstand high growth temperatures, relatively cheap
  - 🙁 Very low thermal conductivity, large lattice mismatch, large CTE mismatch

Coefficient of thermal expansion

- Silicon carbide (SiC)
  - — 
     <sup>(i)</sup> High thermal conductivity, low lattice mismatch, relatively low CTE mismatch
  - 🙁 High cost, crystallographic defects

#### • Silicon (Si)

- — 
   © Low cost, excellent availability of large diameters, acceptable thermal conductivity, processing in standard silicon fabs (high productivity)
- 😕 Large lattice mismatch, very large CTE mismatch



# GaN-on-Si wafers

- Base: silicon substrate with (111) face
- Example recipe:
  - 1. Thin seed layer of AIN
  - Thick buffer layer: superlattice of alternating GaN and AlGaN layers
  - 3. High-quality GaN layer
  - 4. AlGaN barrier
  - 5. GaN cap layer
- Reduce dislocation density
- Stress control / wafer bow





# **Dislocations**

 High initial dislocation density reduced towards surface (2DEG) by optimisation of buffer design



[S. L. Selvaraj et al., Proc. DRC 2012, 53 (2012)]



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#### GaN devices High–electron-mobility transistor (HEMT)

- Ohmic contacts to 2DEG (Ti/AI)
- Source and drain metallisation (AI)
- Gate metal (Ni) on top of GaN cap
  - Schottky contact
- SiN passivation
- Metal field plate(s)



NXP process: [J. J. T. M. Donkers et al., CS-MANTECH 2013, 259]

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#### **GaN devices – HEMT operation**











#### GaN devices Schottky barrier diode (SBD)

- "HEMT without a source"
- "Gate"  $\rightarrow$  **anode** 
  - Longer to handle high current
- "Drain"  $\rightarrow$  cathode





### **GaN devices – diode operation**





- Forward operation (anode+, cathode-)
  - Electrons flow from 2DEG across AlGaN into anode
- Reverse operation
  - Electron leakage from anode edges





# GaN devices – cap layer

- A few extra nanometres of GaN grown on top of AlGaN
- Possible advantages:
  - Decreased reverse leakage through Schottky contact
  - Reduced peak electric field
  - AIGaN protected against processing
  - Nitrogen degassing prevented
  - Increased device gain
  - Increased power added efficiency
  - Improved DC reliability

[P. Waltereit *et al.*, J. Appl. Phys. **106**, 023535 (2009)]
[E. T. Yu *et al.*, Appl. Phys. Lett. **73 (13)**, 1880 (1998)]
[S. Arulkumaran *et al.*, Jpn. J. Appl. Phys. **44**, 2953 (2005)]





## **GaN devices – HEMT characteristics**

- $V_{\rm T}$ : threshold voltage, typically -2 to -4 V
- $V_{\rm F}$ : diode forward turn-on voltage, typically +1 to +2 V



•  $I_{on}$ : on-current, typically taken at  $V_{GS} = 0$  V for  $V_{DS} = 0.1$  V

•  $\Rightarrow$  On-resistance  $R_{\rm on} = V_{\rm DS} / I_{\rm on}$ 



# GaN devices – performance

Johnson's

(rel. to Si

- Wide band gap  $\Rightarrow$  high critical field  $\Rightarrow$  high voltage
- High carrier concentration and velocity  $\Rightarrow$  high current



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#### High frequency

	Si	GaAs	4H-SiC	GaN	Diamond
$E_g$ (eV)	1.1	1.42	3.26	3.39	5.45
$n_i$ (cm <sup>-3</sup> )	$1.5 \times 10^{10}$	$1.5 \times 10^{6}$	8.2×10 <sup>-9</sup>	1.9×10 <sup>-10</sup>	1.6×10 <sup>-27</sup>
Er	11.8	13.1	10	9.0	5.5
$\mu_n$ (cm <sup>2</sup> /Vs)	1350	8500	700	1200(Bulk) 2000(2DEG)	1900
$v_{sat}$ (10 <sup>7</sup> cm/s)	1.0	1.0	2.0	2.5	2.7
E <sub>br</sub> (MV/cm)	0.3	0.4	3.0	3.3	5.6
$\Theta$ (W/cm K)	1.5	0.43	3.3-4.5	1.3	20
$JM = \frac{E_{br}v_{sat}}{2\pi}$	1	2.7	20	27.5	50

[U. K. Mishra et al., Proc. IEEE 96 (2), 287 (2008)]

Suitability for high-frequency power applications

[A. Johnson, RCA Review **26**, 163 (1965)] Stephen Sque - ESSDERC tutorial 16th September 2013

# **GaN devices – performance**

Baliga figure of merit



- Based on minimising the conduction losses in power FETs
- Assumes power losses are solely due to the on-state power dissipation
- Applies to lower frequencies where conduction losses dominate

[B. J. Baliga, Elec. Dev. Lett. 10 (10), 455 (1989)]

Material	$E_g(eV)$	Es	$\mu_n$ (cm <sup>2</sup> /Vs)	$E_c$ (MV/cm)	$v_{sat}(10^7  {\rm cm/s})$	$n_i (cm^{-3})$	<b>BFOM</b> *
Si	1.12	11.8	1350	0.3	1.0	$1.5 \times 10^{10}$	1
GaAs	1.42	13.1	8500	0.4	2.0	$1.8 \times 10^{6}$	17
4H-SiC	3.26	10	720	2.0	2.0	8.2x10 <sup>-9</sup>	134
6H-SiC	2.86	9.7	370	2.4	2.0	$2.4 \times 10^{-5}$	115
2H-GaN	3.44	9.5	900	3.0	2.5	$1.0 \times 10^{-10}$	537

 $E_g$ , bandgap;  $\mathcal{E}_s$ , dielectric constant;  $\mu_n$ , electron mobility;  $E_c$ , critical electric field;  $v_{sal}$ , saturation velocity;  $n_i$ , intrinsic carrier density.

\*BM= $\varepsilon \mu E_c^3$ , BFOM was normalized by the BM of Si.

Sometimes  $E_{g}$  is used!

[N. Ikeda et al., Proc. IEEE 98 (7), 1151 (2010)]



# GaN devices – benchmarking

- Minimise **specific on-resistance**  $(R_{on} \times A)$
- Maximise breakdown voltage





### **GaN devices – benchmarking**

Some more specific-on-resistance vs. breakdown-voltage plots





See also [Q. Jiang *et al.*, EDL **34 (3)**, 357 (2013)] and [Z. Tang *et al.*, EDL **34 (3)**, 366 (2013)] Stephen Sque - ESSDERC tutor

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#### Issues – gate leakage

Various mechanisms potentially involved in gate leakage



[B. S. Eller et al., J. Vac. Sci. Technol. A 31 (5), 050807 (2013)]



See also [L. Xia et al., Appl. Phys. Lett. 102 (11), 113510 (2013)]

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#### **Issues – current collapse**

On-state current temporarily reduced following off-state stress



- Also known as dynamic R<sub>on</sub>
  - On-state resistance depends on recent history of device biasing



#### **Issues – current collapse**

 Device design and substrate composition can have a strong influence on the magnitude of current collapse (dynamic-R<sub>on</sub> increase)



[O. Hilt et al., Proc. ISPSD 2012, 345 (2012)]



Also [S. DasGupta et al., Appl. Phys. Lett. 101 (24), 243506 (2012)]

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#### Issues – virtual-gate effect

#### Off-state stress:

 Electrons from gate injected into trap states next to gate

#### • On-state after stress:

- Trapped electrons act like a negatively biased gate
- 2DEG partially depleted underneath  $\Rightarrow$  increased  $R_{on}$

#### Later (~seconds):

Electrons de-trap,
 2DEG current restored



[R. Vetury *et al.*, Trans. Elec. Dev. **48 (3)**, 560 (2001)] [T. Mizutani *et al.*, TED **50**, 2015 (2003)]

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# Issues – buffer trapping

#### Off-state stress:

 Electrons trapped in bulk (deep donors/acceptors?)

#### • On-state after stress:

Trapped electrons partially deplete the 2DEG above ⇒ increased R<sub>on</sub>

#### Later (~minutes):

Electrons de-trap,
 2DEG current restored

[M. J. Uren *et al.*, Trans. Elec. Dev. **59 (12)**, 3327 (2012)] and refs. therein



[E. Kohn et al., Trans. Microw. Theory Tech. 51 (2), 634 (2003)]

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### Issues – inverse piezoelectric effect

#### Piezoelectric effect:

mechanical stress  $\Rightarrow$  polarisation (*i.e.*, internal electric field)

#### Inverse (or converse) piezoelectric effect:

applied voltage  $\Rightarrow$  electric field  $\Rightarrow$  mechanical stress

[J. Joh et al., Microelec. Reliab. 50 (6), 767 (2010)]

- High field at drain-side edge of gate
  - $\Rightarrow$  local stress  $\Rightarrow$  defect formation
  - $\Rightarrow$  device degradation (reliability)
    - Mitigate with field-plate design  $\rightarrow$
    - Not the full story...
       See [Meneghesso / Meneghini / Zanoni]



[Y. Ando et al., TED 59 (12), 3350 (2012)]



Also [N. A. Mahadik et al., Appl. Phys. Lett. 93 (26), 262106 (2008)]

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### **Breakdown – measurement**

- Typical breakdown measurement:
  - Start with all terminal biases zero
  - Reduce  $V_{\rm G}$  to a few volts below threshold
  - Increase  $V_{\rm D}$  and record terminal currents

 $V_g = V_T$ 

- Current criterion often used for defining breakdown voltage V<sub>br</sub> (*e.g.*, V<sub>DS</sub> for I<sub>D</sub> = 1 mA/mm)
- Other definitions for V<sub>br</sub> used!

L

I,



Drain injection technique: V<sub>S</sub> = 0, set I<sub>D</sub>, sweep V<sub>GS</sub> and find max. V<sub>DS</sub> [S. R. Bahl and J. A. del Alamo, Trans. Elec. Dev. 40 (8), 1558 (1993)]
 [M. Wang and K. J. Chen, Tran. Elec. Dev. 57 (7), 1492 (2010)]



 $I_{d} | V_{d} = 0.05 V$ 

V<sub>T</sub> V<sub>a</sub>

#### Breakdown – mechanisms



- Extrinsic: air arcing, conductive surface layer
- Intrinsic: impact ionisation, punch-through, vertical breakdown



# Breakdown – mechanisms

- Compare terminal currents to assess the relative contributions of different physical mechanisms to breakdown
- Example using current criterion for breakdown:





G

ch (0)

D

(substrate)

G (

 $I_{\rm S}$ 

(0) S

# Breakdown – punch-through

 At high drain biases in the off-state, electrons can travel through the bulk GaN underneath the (turned-off) gate ⇒ drain-to-source current



Prevent using: longer gate, acceptor doping in the bulk, back barrier, ...

[M. J. Uren et al., Trans. Elec. Dev. 53 (2), 395 (2006)]

# **Breakdown – impact ionisation**

 Impact ionisation: high-energy electrons (or holes) can knock other electrons out of valence-band states into conduction-band states, creating electron-hole pairs and hence raising the current



 Avalanche breakdown: every electron (or hole) creates another electron-hole pair, and the current grows uncontrollably



# **Breakdown – impact ionisation**

• Positive temperature coefficient:  $V_{br}$  increases with increasing  $T \Rightarrow$  suggests impact ionisation (increased phonon scattering)

[N. Dyakonova *et al.*, Electron. Lett. **34 (17)**, 1699 (1998)]
[T. Nakao *et al.*, Phys. Stat. Sol. (c) **0 (7)**, 2335 (2003)]
[M. Wang and K. J. Chen, TED **57 (7)**, 1492 (2010)]
[X. Z. Dang *et al.*, Electron. Lett. **35 (7)**, 602 (1999)]
[B. Brar *et al.*, Proc. HPD 2002, 487 (2002)]

 Impact-ionisation parameters for GaN have been evaluated theoretically

[J. Kolník *et al.*, J. Appl. Phys. **81 (2)**, 726 (1997)] [F. Bertazzi *et al.*, J. Appl. Phys. **106**, 063718 (2009)]

…and determined experimentally

[K. Kunihiro et al., EDL 20 (12), 608 (1999)]



Appl. Phys. Lett. **72 (10)**, 2562 (1998)]



Not the full story? See also [Meneghesso / Meneghini / Zanoni]

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## Breakdown – gate-to-drain length scaling

 Breakdown voltage V<sub>br</sub> scales with gate-to-drain length L<sub>GD</sub> until vertical breakdown becomes dominant



• Why is  $\Delta V_{br} / \Delta L_{GD} < 3$  MV/cm? – leakage, electric field peaks, etc....

See also [N. Ikeda et al., Proc. IEEE 98 (7), 1151 (2010)]

## **Breakdown – vertical current**

 Vertical leakage mechanisms / activation energies depend on wafer type [A. Pérez-Tomás *et al.*, J. Appl. Phys. **113**, 174501 (2013)]



Traps identified in carbon-doped GaN-on-Si buffer layers



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[C. Zhou et al., Proc. ISPSD 2012, 245 (2012)]

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# **Breakdown – buffer optimisation**

- Increasing the thickness of the buffer can increase breakdown voltage due to improved material quality and reduced vertical leakage
   [S. L. Selvaraj *et al.*, Elec. Dev. Lett. 33 (10), 1375 (2012)] (see earlier slide)
- The inclusion of a carbon-doped "back barrier" can postpone punchthrough to higher V<sub>DS</sub> (at the expense of increased on-resistance)
   [E. Bahat-Treidel *et al.*, Trans. Elec. Dev. **57 (11)**, 3050 (2010)]
  - [S. A. Chevtchenko et al., Appl. Phys. Lett. 100, 223502 (2012)] ↓





See also [N. Ikeda et al., Proc. IEEE 98 (7), 1151 (2010)]

# **Breakdown – passivation optimisation**

 SiN surface passivation can increase the breakdown voltage by modifying the surface charges/traps (and hence the electric field)





Electroluminescence

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[Y. Ohno et al., Appl. Phys. Lett. 84 (12), 2184 (2004)]

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# Simulation – set-up

- Density gradient vs. classical simulation
- Lattice temperature equation necessary for high-power simulation
- Drift-diffusion vs. hydrodynamic model
- Tunnelling at contacts and interfaces Schottky gate
- Different levels of polarisation models fixed charges vs. built-in polarisation
- Thermionic heterointerface condition
- Mobility models doping dependence, saturation, surface (2DEG) vs. bulk
- Anisotropy? mobility / impact ionisation
- Fermi-Dirac vs. Boltzmann statistics, incomplete ionisation of impurities
- Generation band-to band, impact ionisation
- Recombination direct (band-to-band), Shockley-Read-Hall
- Numerical precision low carrier concentrations, steep gradients



# Simulation – internal observations

- Electron and hole distribution in off-state at high drain bias
  - Can be correlated to (for example) electroluminescence measurements





[Y. Kong et al., Proc. ICMMT 2012, 1]

## Simulation – internal observations



# Simulation – field plates

- There is a large peak in the surface electric field at the drain side of the **gate** (foot)
- Using a gate field plate (head) can reduce this field peak, but adds a new one
- Using another field plate can reduce these peaks but adds a third one



- Field-plate design must be optimised
  - Can affect breakdown, capacitances, current collapse, degradation, etc.

[N.-Q. Zhang et al., Elec. Dev. Lett. 21 (9), 421 (2000)] [J. Li et al., Elec. Lett. 37 (3), 196 (2001)] [A. Wakejima et al., Appl. Phys. Lett. 90, 213504 (2007)]

> [W. Saito et al., Trans. Elec. Dev. 54 (8), 1825 (2007)] [H. Hanawa et al., IRPS 2013, CD.1.1]

# Simulation – field plates

Simulations can be used to optimise the device geometry to obtain the maximum V<sub>br</sub> with minimum degradation in frequency response and R<sub>on</sub> [S. Karmalkar and U. K. Mishra, Trans. Elec. Dev. 48 (8), 1515 (2001)]





## Simulation – field plates

- Making the gate-connected field plate too long can reduce  $V_{\rm br}$ 
  - Depending on definition of  $V_{\rm br}!$



[H. Onodera and K. Horio, Proc. EMICC (EuMIC) 2012, 401]



#### Simulation – comparison to measurements

 Kelvin probe force microscopy used to map internal potential distribution (w/wo FP)

[A. Wakejima et al., Appl. Phys. Lett. 90, 213504 (2007)]





See also [S. Kamiya et al., Appl. Phys. Lett. 90, 213511 (2007)]

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<sup>12</sup>V 15 V

D

10

S

# Simulation – drain field peak?

- Electric field peak at drain at very high voltage – enough to cause breakdown?
  - Dependent on specific details of Ohmic-contact implementation?





# Simulation – impact ionisation

- Improved modelling of impact ionisation can have a significant effect on simulated breakdown voltages
  - Treat impact-ionisation parameters as tuning parameters





107

1**0**6

**10**5

104

10<sup>3</sup>

10<sup>2</sup>

10<sup>1</sup>

rigorous model

2

3

Impact ionization coefficient (cm<sup>-1</sup>)

[K. Kodama et al., J. Appl. Phys. **114**, 044509 (2013)]

# Simulation – buffer optimisation

 Thinning the lowly doped "spacing layer" between surface and carbon-doped layer can increase breakdown voltage via a decrease in the surface electric field peak



See also [M. J. Uren et al., Trans. Elec. Dev. 59 (12), 3327 (2012)]

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ata from Gan IGHEMT-AlGan Vg-30 Vd300 spacer0.5um Ver1-R9.

Spacing layer

Gate

0.5

 $V_{\rm D} = 300 \ {\rm V}$ 

# Simulation – multiphysics

- Thermo-electro-elastic simulations:
  - fully coupled thermal, mechanical, and electrical equations
- Used to investigate (for example):
  - The role of thermal and piezoelectric stresses on defect formation
  - ...and the impact on electrical characteristics



[M. G. Ancona *et al.*, J. Appl. Phys. **111**, 074504 (2012)] [M. G. Ancona, Proc. IEDM 2012, 315]

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**TEM** [U. Chowdhury *et al.*, EDL **29 (10)**, 1098 (2008)]

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# Modelling – compact models

- Models for GaN devices are needed to enable application development via circuit simulation and optimisation
- Different types of compact model:
  - Table-based: measured device data stored in large look-up tables
    - Very fast, but extrapolation outside of measured range is treacherous, and accurate scaling to other device dimensions is not possible
  - Empirical: uses whichever mathematical functions have the right shape
    - Good fits possible, but parameters are not physically meaningful, scaling is not physical, and extrapolation is still dubious
  - Physics-based: equations derived from modelling physical phenomena
    - Parameters physically meaningful, scaling is physical, extrapolation reliable
    - Threshold-voltage-based: physical expressions smoothed together
    - Surface-potential-based: uses a single expression for all regimes, inherent symmetry, established as the preferred approach in MOS modelling [Gildenblat *et al.*, J. Solid-State Circ. **39 (9)**, 1394 (2004)]



See also [L. Dunleavy et al., Microwave Magazine 11 (6), 82 (2010)] PUBLIC 63

# Modelling – empirical model

#### Chalmers (a.k.a. Angelov) model

- An empirical model for HEMT and MESFET devices, introduced in 1992
   [I. Angelov *et al.*, Trans. Micro. Theory. Tech. 40 (12), 2258 (1992)]
- Extended in 1996 to include temperature, dispersion, and soft breakdown
   [I. Angelov et al., TMTT 44 (10), 1664 (1996)]
- Widely used for (RF) GaN-HEMTs
- Modified in 2010 to make parameters more physical

[T. Oishi et al., Proc. INMMIC 2010, 20 (2010)]



[I. Angelov *et al.*, Proc. MTT 2012, 1 (2012)] [I. Angelov *et al.*, Proc. APMC 2006, 279]

# Modelling – empirical model

Modified form of the Angelov model for GaN-on-Si power switches



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[S. Stoffels *et al.*, Proc. THERMINIC 2011, 1 (2011)] See also [S. Stoffels THERMINIC 2012] Stephen Sque - E



[A. Koudymov et al., Trans. Elec. Dev. 55 (3), 712 (2008)]

# Modelling – physics-based model

 Model for 2DEG charge density: [S. Khandelwal *et al.*, Trans. Elec. Dev. 58 (10), 3622 (2011)]

$$n_s = \frac{C_g V_{\rm go}}{q} \frac{V_{\rm go} + V_{\rm th} \left[1 - \ln(\beta V_{\rm gon})\right] - \frac{\gamma_0}{3} \left(\frac{C_g V_{\rm go}}{q}\right)^{2/3}}{V_{\rm go} \left(1 + \frac{V_{\rm th}}{V_{\rm god}}\right) + \frac{2\gamma_0}{3} \left(\frac{C_g V_{\rm go}}{q}\right)^{2/3}}$$

Expression extended for validity in sub-threshold regime...

$$n_{s,unified} = \frac{2V_{th}(C_g/q)\ln\{1 + \exp(V_{go}/2V_{th})\}}{1/H(V_{go,p}) + (C_g/qD)\exp(-V_{go}/2V_{th})}$$

...and used as basis for drain-current model...

Smoothly 
$$\begin{bmatrix} I_{d,abo\,ve} = \frac{\mu_0 C_g W_g}{L_g G_{mob} G_{field}} \left\{ \sum_{i=1}^6 c_i \{\psi_{gd}^i - \psi_{gs}^i\} + c_0 \ln\left(\frac{\psi_{gd}}{\psi_{gs}}\right) \right\} \\ I_{d,sub} = \frac{2\mu_0 W_g q D V_{th}^2}{L_g G_{mob} G_{field}} \exp\left(\frac{V_{go}}{V_{th}}\right) \left(1 - \exp\left(\frac{-V_{ds}}{V_{th}}\right)\right) \end{bmatrix}$$

...to which carrier velocity saturation, channel-length modulation, short-channel effects, and self-heating are added



[S. Khandelwal and T. A. Fjeldly, Solid-State Electronics **76**, 60 (2012)] See also [Yigletu *et al.*, Proc. WiSNet / SiRF / RWS / PAWR 2013]

See also [U. Radhakrishna *et al.*, Proc. IEDM 2012, 319/13.6.1 (2012)] and [X. Cheng *et al.*, TED **56**, 2881 (2009)] Stephen Sque - ESSDERC tutorial 16th September 2013

# Modelling – physics-based model

- "Zone-based" compact model based on observations from device simulations
  - Different equations derived for different regions of the device, then smoothly joined
  - Alternative to equivalent-circuit models



Field (V/cm

ateral Electric Field (Ex

[H. Yin et al., Proc. IMS 2007, 787 and Proc. IMS 2008, 1425] and [D. Hou et al., TED 60 (2), 639 (2013)] Stephen Sque - ESSDERC tutorial 16th September 2013 PUBLIC 68

# Modelling – surface-potential–based model

The "first surface-potential-based compact model for RF GaN HEMTs"



[D. L. John et al., Proc. IEDM 2010, 186/8.3.1 (2010)]

### Modelling – surface-potential-based model

 A Surface-Potential-Based Compact Model for AlGaN/GaN MODFETs [X. Cheng and Y. Wang, Trans. Elec. Dev. 58 (2), 448 (2011)]



Analytical Modeling of Surface-Potential and Intrinsic Charges in AlGaN/GaN HEMT Devices
 [S. Khandelwal et al., Trans. Elec. Dev. 59 (10), 2856 (2012)] and unpub. Trans. Elec. Dev.

$$n_{s} = DV_{\text{th}} \left[ \ln \left( 1 + e^{\frac{E_{f} - E_{0}}{V_{\text{th}}}} \right) + \ln \left( 1 + e^{\frac{E_{f} - E_{1}}{V_{\text{th}}}} \right) \right]$$

$$E_{0,1} = \gamma_{0,1} n_{s}^{2/3} \qquad n_{s} = \frac{\epsilon}{qd} (V_{\text{go}} - E_{f} - V_{x})$$

$$I_{\text{ds}} = \frac{\mu_{\text{eff}} C_{g}}{\sqrt{1 + \theta_{\text{sat}}^{2} \psi_{\text{ds}}^{2}}} \frac{W}{L} \left( V_{\text{go}} - \psi_{m} + V_{\text{th}} \right) (\psi_{\text{ds}}) \left( 1 + \lambda V_{\text{ds}} \right)$$

$$D_{\text{rin Voltage (Volts)}}$$



See also [R. Jana and D. Jena, Proc. DRC 2012, 147 (2012)] and [Martin / Hahe / Lucci (2012–2013)] Stephen Sque - ESSDERC tutorial 16th September 2013

#### Outline

- GaN and related materials
- The AlGaN/GaN heterostructure
- GaN wafers
- GaN devices
- Issues facing high-voltage GaN-HEMT development
- High-voltage breakdown
- GaN-HEMT device simulation
- Compact modelling of GaN HEMTs
- Summary and conclusion



## Summary and conclusion

- The material properties of GaN and AlGaN, together with the remarkable properties of the AlGaN/GaN heterostructure, enable the creation of high-power, high-frequency devices
- Issues affecting AIGaN/GaN-based device development include: leakage currents, current collapse (dynamic behaviour), reliability, and sub-optimal breakdown
- Device simulation can be used to explore and address these issues, for example through buffer-composition and field-plate optimisation
- **Compact models** for GaN HEMTs are maturing into surface-potential– (physics-) based models with high accuracy, efficiency, and scalability (the Compact Model Council is currently choosing a standard GaN-HEMT compact model)


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